

CLAIMS

What is claimed is:

- 1 1. An apparatus for inserting one or more data bytes into a stream of data  
2 words, comprising:  
3 a first circuit to generate a first and a second intermediate data word  
4 correspondingly containing first and second zero or more data bytes of a first data  
5 word of a preceding cycle, said first and second zero or more data bytes being data  
6 bytes that precede and follow a first data byte insertion point of the preceding cycle  
7 respectively, and said first and second zero or more data bytes being repositioned  
8 within said first and second intermediate data words respectively, with said first zero  
9 or more data bytes being repositioned within said first intermediate data word  
10 relative to cascaded alignment impact of cycles prior to said preceding cycle, and  
11 said second zero or more data bytes being repositioned within said second  
12 intermediate data word relative to said cascaded alignment impact of cycles prior to  
13 said preceding cycle, said first data byte insertion point of the preceding cycle, and a  
14 first number of data bytes inserted after said first data byte insertion point of the  
15 preceding cycle;  
16 a second circuit to generate a first re-aligned variant of a first insertion data  
17 word containing said first number of data bytes inserted during said preceding cycle;  
18 and  
19 a third circuit coupled to said first and second circuits to generate an output  
20 data word conditionally using selected parts of said first and second intermediate  
21 data words, and said first re-aligned variant of the first insertion data word.

1 2. The apparatus of claim 1, wherein said first circuit comprises an arithmetic  
2 operator, a first and a second logic operator, a first selector coupled to said first logic  
3 operator, and a second selector coupled to said arithmetic operator and said second  
4 logic operator to generate a first position pointer pointing to a first data byte position  
5 after which said data byte insertion of the preceding cycle began, and a second  
6 position pointer pointing to a second data byte position at which said data byte  
7 insertion of the preceding cycle ended, respectively.

1 3. The apparatus of claim 1, wherein  
2 said apparatus further comprises a register to store a shift amount for  
3 shifting said first data word of the preceding cycle to generate said first intermediate  
4 data word with said first zero or more data bytes before said first data byte insertion  
5 point of the preceding cycle repositioned relative to cascaded alignment impact of  
6 cycles prior to said preceding cycle; and

7 said first circuit comprises an arithmetic operator and a selector coupled to  
8 the arithmetic operator to generate a second shift amount for shifting said first data  
9 word of the preceding cycle to generate said second intermediate data word with  
10 said second zero or more data bytes after said first data byte insertion point of the  
11 preceding cycle repositioned relative to said cascaded alignment impact of cycles  
12 prior said preceding cycle, said first data byte insertion point of the preceding cycle,  
13 and said first number of data bytes inserted after said first data byte insertion point of  
14 the preceding cycle.

1 4. The apparatus of claim 1, wherein said first circuit further comprises a bit  
2 concatenator, a plurality of arithmetic operators, and a plurality of shifters  
3 correspondingly coupled to the concatenator and the arithmetic operators to

- 4 generate said first and second intermediate data words with said first and second  
5 zero or more data bytes repositioned accordingly.

1 5. The apparatus of claim 1, wherein said second circuit comprises a  
2 concatenator and a shifter coupled to the concatenator to generate said re-aligned  
3 variant of said first insertion data word containing said first number of data bytes  
4 inserted.

1 6. The apparatus of claim 1, wherein said third circuit comprises data bit  
2 selection logic that conditionally selects data bits from said first and second  
3 intermediate data words and said first re-aligned variant of the first insertion data  
4 word to form said output data word.

1 7. The apparatus of claim 6, wherein said selection logic conditionally selects  
2 data bits from said first and second intermediate data words and said first re-aligned  
3 variant of the first insertion data word to form said output data word, in accordance  
4 with a plurality of multi-bit data bit selection masks.

1 8. The apparatus of claim 7, wherein said selection logic conditionally selects a  
2 data bit from said first intermediate data word if the corresponding data bits of said  
3 data bit selection masks form a "110" data bit pattern, from said second intermediate  
4 data word if the corresponding data bits of said data bit selection masks form a "101"  
5 data bit pattern, and from said first re-aligned variant of the first insertion data word if  
6 the corresponding data bits of said data bit selection masks form a "100" data bit  
7 pattern.

1 9. The apparatus of claim 1, wherein said apparatus further comprises one or  
2 more registers for storing at least a selected one of said first data word, a first shift  
3 amount said first data word was shifted to accommodate cascaded alignment impact  
4 of cycles prior to said preceding cycle, a second shift amount said first data word  
5 was shifted to accommodate cascaded alignment impact of cycles prior to said  
6 preceding cycle and said first number of data bytes inserted after said first data byte  
7 insertion point of the preceding cycle, a first data byte position after which said first  
8 number of data bytes of the preceding cycle was inserted, a second data byte  
9 position at which insertion of said first number of data bytes of the preceding cycle  
10 ended, and an overflow indicator indicating an insertion overflow condition.

1 10. The apparatus of claim 1, wherein the apparatus further comprises fourth  
2 circuitry to generate a plurality of multi-bit data bit selection masks for use by said  
3 third circuitry in forming said output data word, conditionally using selected parts of  
4 said first and second intermediate data words, and said first re-aligned variant of the  
5 first insertion data word.

1 11. The apparatus of claim 10, wherein said fourth circuitry comprises a plurality  
2 of shifters, a first plurality of logical operators correspondingly coupled to selected  
3 ones of said shifters, and a second plurality of logical operators correspondingly  
4 coupled to selected ones of said first logical operators for generating said multi-bit  
5 data bit selection masks.

1 12. The apparatus of claim 1, wherein  
2 a fourth circuit to generate a third and a fourth intermediate data word  
3 correspondingly containing third and fourth zero or more data bytes of a second data  
4 word of a current cycle, said third and fourth zero or more data bytes being data

5 bytes that precede and follow a second data byte insertion point of the current cycle  
6 respectively, and said third and fourth zero or more data bytes being repositioned  
7 within said third and fourth intermediate data words respectively, with said third zero  
8 or more data bytes being repositioned within said third intermediate data word  
9 relative to cascaded alignment impact of cycles prior to said current cycle, and said  
10 fourth zero or more data bytes being repositioned within said fourth intermediate  
11 data word relative to said cascaded alignment impact of cycles prior to said current  
12 cycle, said second data byte insertion point of the current cycle, and a second  
13 number of data bytes to be inserted after said data byte insertion point of the current  
14 cycle;

15 a fifth circuit to generate a second re-aligned variant of a second insertion  
16 data word containing said second number of data bytes of the current cycle to be  
17 inserted; and

18 said third circuit is also coupled to said third and fourth circuits, and  
19 conditionally uses selected parts of said third and fourth intermediate data words,  
20 and said second re-aligned variant of the second insertion data word to generate  
21 said output data word.

1 13. The apparatus of claim 12, wherein said fourth circuit comprises a plurality of  
2 arithmetic operators selectively coupled to each other in a pre-determined manner to  
3 generate a first position pointer pointing to a first data byte position after which said  
4 second data byte insertion of the current cycle began, and a second position pointer  
5 pointing to a second data byte position at which said second data byte insertion of  
6 the current cycle ended, respectively.

1 14. The apparatus of claim 12, wherein  
2 said apparatus further comprises a register to store a shift amount for  
3 shifting said second data word of the current cycle to generate said third  
4 intermediate data word with said third zero or more data bytes before said second  
5 data byte insertion point of the current cycle repositioned relative to cascaded  
6 alignment impact of cycles prior to said current cycle; and  
7 said fourth circuit comprises an arithmetic operator coupled to the register to  
8 generate a second shift amount for shifting said second data word of the current  
9 cycle to generate said fourth intermediate data word with said fourth zero or more  
10 data bytes after said second data byte insertion point of the current cycle  
11 repositioned relative to said cascaded alignment impact of cycles prior to said  
12 current cycle, said second data byte insertion point of the current cycle, and said  
13 second number of data bytes inserted after said second data byte insertion point of  
14 the current cycle.

1 15. The apparatus of claim 12, wherein said fourth circuit further comprises a  
2 plurality of arithmetic operators and a plurality of shifters correspondingly coupled to  
3 the arithmetic operators to generate said third and fourth intermediate data words  
4 with said third and fourth zero or more data bytes repositioned accordingly.

1 16. The apparatus of claim 12, wherein said fifth circuit comprises a shifter to  
2 generate said re-aligned variant of said second insertion data word of the current  
3 cycle, containing said second number of data bytes of the current cycle to be  
4 inserted.

1 17. The apparatus of claim 12, wherein said third circuit comprises data bit  
2 selection logic that conditionally selects data bits from said third and fourth  
3 intermediate data words and said second re-aligned variant of the second insertion  
4 data word to form said output data word.

1 18. The apparatus of claim 17, wherein said selection logic conditionally selects  
2 data bits from said third and fourth intermediate data words and said second re-  
3 aligned variant of the second insertion data word to form said output data word, in  
4 accordance with a plurality of multi-bit data bit selection masks.

1 19. The apparatus of claim 18, wherein said selection logic conditionally selects a  
2 data bit from said third intermediate data word if the corresponding data bits of said  
3 data bit selection masks form a "010" data bit pattern, from said fourth intermediate  
4 data word if the corresponding data bits of said data bit selection masks form a "001"  
5 data bit pattern, and from said second re-aligned variant of the second insertion data  
6 word if the corresponding data bits of said data bit selection masks form a "000" data  
7 bit pattern.

1 20. The apparatus of claim 12, wherein the apparatus further comprises sixth  
2 circuitry to generate a plurality of multi-bit data bit selection masks for use by said  
3 third circuitry in forming said output data word, conditionally using selected parts of  
4 said third and fourth intermediate data words, and said second realigned variant of  
5 the second insertion data word.

1 21. The apparatus of claim 20, wherein said sixth circuitry comprises a plurality of  
2 shifters, a first plurality of logical operators correspondingly coupled to selected ones  
3 of said shifters, and a second plurality of logical operators correspondingly coupled

4 to selected ones of said first logical operators for generating said multi-bit data bit  
5 selection masks.

1 22. The apparatus of claim 1, wherein the apparatus is a selected one of an  
2 application specific integrated circuit, a micro-controller, a digital signal processor, a  
3 general purpose microprocessor, and a network processor.

1 23. An apparatus for inserting one or more data bytes into a stream of data  
2 words, comprising:

3 a first circuit to generate a first and a second intermediate data word  
4 correspondingly containing first and second zero or more data bytes of a first data  
5 word of a current cycle, said first and second zero or more data bytes being data  
6 bytes that precede and follow a first data byte insertion point of the current cycle  
7 respectively, and said first and second zero or more data bytes being repositioned  
8 within said first and second intermediate data words respectively, with said first zero  
9 or more data bytes being repositioned within said first intermediate data word  
10 relative to cascaded alignment impact of cycles prior to said current cycle, and said  
11 second zero or more data bytes being repositioned within said second intermediate  
12 data word relative to said cascaded alignment impact of cycles prior to said current  
13 cycle, said first data byte insertion point of the current cycle, and a first number of  
14 data bytes to be inserted after said first data byte insertion point of the current cycle;  
15 a second circuit to generate a first re-aligned variant of a first insertion data  
16 word containing said first number of data bytes to be inserted during said current  
17 cycle; and  
18 a third circuit coupled to said first and second circuits to generate an output  
19 data word conditionally using selected parts of said first and second intermediate  
20 data words, and said first re-aligned variant of the first insertion data word.



1 24. The apparatus of claim 23, wherein said first circuit comprises a plurality of  
2 arithmetic operators selectively coupled to each other in a pre-determined manner to  
3 generate a first position pointer pointing to a first data byte position after which said  
4 second data byte insertion of the current cycle began, and a second position pointer  
5 pointing to a second data byte position at which said second data byte insertion of  
6 the current cycle ended, respectively.

1 25. The apparatus of claim 23, wherein  
2 said apparatus further comprises a register to store a shift amount for  
3 shifting said first data word of the current cycle to generate said first intermediate  
4 data word with said first zero or more data bytes before said first data byte insertion  
5 point of the current cycle repositioned relative to cascaded alignment impact of  
6 cycles prior to said current cycle; and  
7 said first circuit comprises an arithmetic operator coupled to the register to  
8 generate a second shift amount for shifting said first data word of the current cycle to  
9 generate said second intermediate data word with said second zero or more data  
10 bytes after said first data byte insertion point of the current cycle repositioned  
11 relative to said cascaded alignment impact of cycles prior to said current cycle, said  
12 first data byte insertion point of the current cycle, and said first number of data bytes  
13 inserted after said first data byte insertion point of the current cycle.

1 26. The apparatus of claim 23, wherein said first circuit further comprises a  
2 plurality of arithmetic operators and a plurality of shifters correspondingly coupled to  
3 the arithmetic operators to generate said first and second intermediate data words  
4 with said first and second zero or more data bytes repositioned accordingly.

1 27. The apparatus of claim 23, wherein said second circuit comprises a shifter to  
2 generate said re-aligned variant of said first insertion data word of the current cycle,  
3 containing said first number of data bytes of the current cycle to be inserted.

1 28. The apparatus of claim 23, wherein said third circuit comprises data bit  
2 selection logic that conditionally selects data bits from said first and second  
3 intermediate data words and said first re-aligned variant of the first insertion data  
4 word to form said output data word.

1 29. The apparatus of claim 28, wherein said selection logic conditionally selects  
2 data bits from said first and second intermediate data words and said first re-aligned  
3 variant of the first insertion data word to form said output data word, in accordance  
4 with a plurality of multi-bit data bit selection masks.

1 30. The apparatus of claim 29, wherein said selection logic conditionally selects a  
2 data bit from said first intermediate data word if the corresponding data bits of said  
3 data bit selection masks form a "010" data bit pattern, from said second intermediate  
4 data word if the corresponding data bits of said data bit selection masks form a "001"  
5 data bit pattern, and from said first re-aligned variant of the first insertion data word if  
6 the corresponding data bits of said data bit selection masks form a "000" data bit  
7 pattern.

1 31. The apparatus of claim 23, wherein the apparatus further comprises fourth  
2 circuitry to generate a plurality of multi-bit data bit selection masks for use by said  
3 third circuitry in forming said output data word, conditionally using selected parts of  
4 said first and second intermediate data words, and said first realigned variant of the  
5 first insertion data word.

1 32. The apparatus of claim 31, wherein said fourth circuitry comprises a plurality  
2 of shifters, a first plurality of logical operators correspondingly coupled to selected  
3 ones of said shifters, and a second plurality of logical operators correspondingly  
4 coupled to selected ones of said first logical operators for generating said multi-bit  
5 data bit selection masks.

1 33. The apparatus of claim 23, wherein the apparatus is a selected one of an  
2 application specific integrated circuit, a micro-controller, a digital signal processor, a  
3 general purpose microprocessor, and a network processor.

1 34. An apparatus for inserting one or more data bytes into a stream of data  
2 words, comprising:  
3 a first circuit to generate a plurality of multi-bit data bit selection masks; and  
4 a second circuit coupled to said first circuit to generate an output data word  
5 conditionally using selected parts of a first and a second intermediate data word  
6 generated from a first input data word of a current cycle, a third and a fourth  
7 intermediate data word generated from a second input data word of a preceding  
8 cycle, a first re-aligned variant of a first insertion data word of the current cycle, and  
9 a second re-aligned variant of a second insertion data word of the preceding cycle,  
10 in accordance with said data bit selection masks.

1 35. The apparatus of claim 34, wherein second circuit comprises selection logic  
2 that conditionally selects a data bit from said first intermediate data word if the  
3 corresponding data bits of said data bit selection masks form a "010" data bit  
4 pattern, from said second intermediate data word if the corresponding data bits of  
5 said data bit selection masks form a "001" data bit pattern, and from said first re-

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6 aligned variant of the first insertion data word if the corresponding data bits of said  
7 data bit selection masks form a "000" data bit pattern.

1 36. The apparatus of claim 34, wherein said second circuit comprises selection  
2 logic that conditionally selects a data bit from said third intermediate data word if the  
3 corresponding data bits of said data bit selection masks form a "110" data bit  
4 pattern, from said fourth intermediate data word if the corresponding data bits of said  
5 data bit selection masks form a "101" data bit pattern, and from said second re-  
6 aligned variant of the second insertion data word if the corresponding data bits of  
7 said data bit selection masks form a "100" data bit pattern.

1 37. The apparatus of claim 34, wherein said first circuitry comprises a plurality of  
2 shifters, a first plurality of logical operators correspondingly coupled to selected ones  
3 of said shifters, and a second plurality of logical operators correspondingly coupled  
4 to selected ones of said first logical operators for generating said multi-bit data bit  
5 selection masks.

1 38. The apparatus of claim 34, wherein the apparatus is a selected one of an  
2 application specific integrated circuit, a micro-controller, a digital signal processor, a  
3 general purpose microprocessor, and a network processor.